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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/612,281	TAGGART ET AL.
	Examiner	Art Unit
	Jeremy C. Norris	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-9, 17-21, and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,252,178 B1 (Hashemi).

Hashemi discloses, referring primarily to figure 2a, an article comprising: a wire-bonding mounting substrate (210) including a first surface and a second surface; a first wire-bond pad (240) disposed upon the first surface; and a first via (230) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad [claim 1], wherein the via includes a liner that is electrically conductive (col. 3, lines 60-66) [claim 3], further including: an interconnect (260) filling the via [claim 4], wherein the via includes a liner (col. 3, lines 60-66), further including; an interconnect (260) filling the via [claim 5], wherein the wire-bond pad includes a first layer and a second layer, wherein at least one of the first layer and the second layer is selected from a precious metal, a precious metal alloy, silver, gold, platinum, nickel, palladium, platinum, cobalt, rhodium, iridium, and combinations thereof (col. 4, lines 15-20) [claim 6], wherein the wire-bond pad includes a first layer and a second layer, and

wherein the second layer is one of identical material to the first layer, or at least one of a more noble, or a softer metal than the first layer (col. 4, lines 15-20) [claim 7].

Similarly, Hashemi discloses, referring primarily to figure 2a, a package comprising: a wire-bonding mounting substrate (210) including a first surface and a second surface; a first wire-bond pad (240) disposed upon the first surface; a first via (230) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad; a die (270) disposed on the first surface; and a first wire bond (280) that couples the die to the first wire-bond pad [claim 8], further including: a second wire-bond pad disposed upon the first surface; a second via in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad (col. 4, lines 15-20) [claim 9].

Additionally, Hashemi discloses, referring primarily to figure 2a, a process comprising: forming a first via (230) in a wire-bonding mounting substrate (210), wherein the wire- bonding mounting substrate includes a first surface and a second surface, and wherein forming proceeds from the second surface toward the first surface; and patterning a first wire-bond pad (240) symmetrically and directly over the first via [claim 17], wherein forming ceases upon contact with the first wire-bond pad [claim 18], further including: forming a via liner (col. 3, lines 60-68) in the first via [claim 19], further including: filling the first via with an interconnect (260) [claim 20], wherein forming the first via precedes patterning the first wire-bond pad (figures 2c-d) [claim 21].

Furthermore, Hashemi discloses, referring primarily to figure 2a, a method comprising: forming a first via (230) in a wire-bonding mounting substrate (210), wherein the wire-bonding mounting substrate includes a first surface and a second surface, and wherein forming proceeds from the second surface toward the first surface', patterning a first wire-bond pad (240) directly over the first via; and coupling a die (270) to the first wire-bond pad [claim 24], further including: forming a second via in the wire-bonding mounting substrate; patterning a second wire-bond pad directly over the second via; and coupling the die to the second wire-bond pad (col. 4, lines 15-20) [claim 25], further including: filling the first via with an interconnect (260) [claim 26].

Claims 2, 8-12, 14-18, and 20-27 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,084,295 (Horiuchi).

Horiuchi discloses, referring primarily to figures 4 and 5, an article comprising: a wire-bonding mounting substrate (5) including a first surface and a second surface; a first wire-bond pad (22) disposed upon the first surface; and a first via (36) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed directly below the first wire-bond pad, wherein the wire-bonding mounting substrate includes a first edge, the article further including: a second wire-bond pad (22) disposed upon the first surface; a second via (36) in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad; and wherein the first via and the second via are

staggered with respect to the first edge of the wire-bonding mounting substrate (figure 4) [claim 2].

Similarly, Horiuchi discloses, referring primarily to figures 4-5, a package comprising: a wire-bonding mounting substrate (5) including a first surface and a second surface; a first wire-bond pad (22) disposed upon the first surface; a first via (36) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad; a die (10) disposed on the first surface; and a first wire bond (20) that couples the die to the first wire-bond pad [claim 8], further including: a second wire-bond pad (22) disposed upon the first surface; a second via (36) in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad [claim 9], further including: a second wire-bond pad (22) disposed upon the first surface; a second via (36) in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad; a second bond wire (20) that couples the die to the second wire-bond pad; and wherein the respective lengths of the first bond wire and the second bond wire are adjusted so as to tune the package (col. 5, lines 50-60) [claim 10], further including: a first bump (12) coupled to the first via [claim 11], further including: a first bump (12) coupled to the first via; and a first trace (24) that makes an electrical contact to the first bump [claim 12], wherein the first wire-bond pad is part of a plurality of wire-bond pads, and wherein

each wire-bond pad is directly above a corresponding via from a plurality of vias (figure 5) [claim 14], wherein the first wire-bond pad is part of a plurality of wire-bond pads, wherein each wire-bond pad is directly above a corresponding via from a plurality of vias, and wherein each via is coupled to a bump (figure 5) [claim 15], wherein the first wire-bond pad is part of a plurality of wire-bond pads, wherein each wire-bond pad is directly above a corresponding via from a plurality of vias, wherein each via is coupled to a bump, and wherein each bump is directly below a corresponding via (figure 5) [claim 16].

Also, Horiuchi discloses, referring primarily to figures 4-5, a process comprising: forming a first via (36) in a wire-bonding mounting substrate (5), wherein the wire-bonding mounting substrate includes a first surface and a second surface, and wherein forming proceeds from the second surface toward the first surface; and patterning a first wire-bond pad (22) symmetrically and directly over the first via [claim 17], wherein forming ceases upon contact with the first wire-bond pad [claim 18], further including: filling the first via with an interconnect (18) [claim 20], wherein forming the first via precedes patterning the first wire-bond pad (col. 6, lines 1-10) [claim 21], further including: filling the first via with an interconnect (18); coupling the first via to a first bump (12) [claim 22], further including: coupling the first wire-bond pad to a first bump (12) [claim 23].

Furthermore, Horiuchi discloses, referring primarily to figures 4-5, a method comprising: forming a first via (36) in a wire-bonding mounting substrate (5), wherein the wire-bonding mounting substrate includes a first surface and a second surface, and

wherein forming proceeds from the second surface toward the first surface; patterning a first wire-bond pad (22) directly over the first via; and coupling a die (10) to the first wire-bond pad [claim 24], further including: forming a second via (36) in the wire-bonding mounting substrate; patterning a second wire-bond pad (22) directly over the second via; and coupling the die to the second wire-bond pad [claim 25], further including: filling the first via with an interconnect (18) [claim 26], further including: filling the first via with an interconnect (18); and coupling the first via to a first bump (12) [claim 27].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi in view of US 5,936,844 (Walton).

Regarding claim 13, Horiuchi discloses the claimed invention as described above with respect to claim 8 including a first bump (12) coupled to the first via. Horiuchi does not specifically disclose a larger substrate coupled to the first bump [claim 13]. However, it is well known in the art to attach a BGA semiconductor device to a larger substrate via a bump as evidenced by Walton (figure 11B). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to attach the semiconductor device of Horiuchi to a larger substrate via the first bump as is known in the art and evidenced by Walton. The motivation for doing so would have been to transmit signals from the die to the larger substrate.

Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walton in view of Horiuchi.

Walton discloses, referring primarily to figures 11A-B, 28. a computing system comprising: a semiconductor device (232) having a die and dynamic random-access memory (162) coupled to the die. Walton does not specifically disclose that the

semiconductor device comprises a wire-bonding mounting substrate including a first surface and a second surface; a first wire-bond pad disposed upon the first surface; a first via in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad; a die disposed on the first surface [claim 28]. Horiuchi discloses, a semiconductor device comprising: a wire-bonding mounting substrate (5) including a first surface and a second surface; a first wire-bond pad (22) disposed upon the first surface; a first via (18) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad; a die (10) disposed on the first surface. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use the semiconductor device taught by Horiuchi as the semiconductor device in the invention of Walton. The motivation for doing so would have been to use a semiconductor device with improved electrical characteristics (Horiuchi – col. 5, lines 50-60).

Moreover, the modified invention of Walton teaches, wherein the computing system is disposed in one of a computer, a wireless communicator, a hand-held device, an automobile, a locomotive, an aircraft, a watercraft, and a spacecraft (Walton – col. 4, lines 50-55) [claim 29], wherein the die is selected from a data storage device, a digital signal processor, a micro controller, an application specific integrated circuit, and a microprocessor (Walton – col. 5, lines 30-40) [claim 30].

Response to Arguments

Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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